

1 **STRUCTURE AND METHOD TO FORM SOURCE AND DRAIN REGIONS**
2 **OVER DOPED DEPLETION REGIONS**

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4 **ABSTRACT**

5 A structure and method of reducing junction capacitance of a
6 source/drain region in a transistor. A gate structure is formed over on a first conductive
7 type substrate. We perform a doped depletion region implantation by implanting ions
8 being the second conductive type to the substrate using the gate structure as a mask, to
9 form a doped depletion region beneath and separated from the source/drain regions. The
10 doped depletion regions have an impurity concentration and thickness so that the doped
11 depletion regions are depleted due to a built-in potential creatable between the doped
12 depletion regions and the substrate. The doped depletion region and substrate form
13 depletion regions between the source/drain regions and the doped depletion region. We
14 perform a S/D implant by implanting ions having a second conductivity type into the
15 substrate to form S/D regions. The doped depletion region and depletion regions reduce
16 the capacitance between the source/drain regions and the substrate.

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